REMARKS

The Office Action dated April 4, 2005 has been received and the Examiner's comments carefully reviewed. Prior to entry of this paper, Claims 1-20 were pending. Claims 1-5 and 8-20 were rejected, and Claims 6 and 7 were allowed. In this paper, Claims 1, 8, 9, 11, 13, 17, and 20 are amended. Claims 1-20 are currently pending. No new subject matter has been added. For at least the following reasons, Applicant respectfully submits that each of the presently pending claims is in condition for allowance.

Rejection to Claims 1, 3-5, 9, 10, 12, and 17-19

Claim 1 is amended in this paper. The rejection to Claims 1 and 10 are respectfully traversed. It is respectfully submitted that Applicant's Claim 1 as amended is allowable at least because the Nebel does not disclose, "the second shunt circuit is arranged to short the low-range node to the second bias node if a voltage associated with the full-range node corresponds to a logic high", as recited in Applicant's Claim 1 as amended. Also, it is respectfully submitted that Applicant's Claim 10 is allowable at least because Nebel does not disclose, "the first shunt circuit is configured to short the first bias node to the high-range node if the full-range signal corresponds to a logic low", as recited in Applicant's Claim 10.

With regard to Claim 10, the Office Action states, with regard to the circuit illustrated in Fig. 1 of Nebel, "the first shunt circuit (MP21-MP22) is configured to short (connect or conduct) the first bias node (5) from the high-range node (P1) if the full-range signal (IN) corresponds to a logic low (logic 0)." Applicant respectfully disagrees.

In Nebel, node 5 is at the gate of MOSFET MP22, and node P1 is at the gate of MOSFET MP21. In Nebel, when signal IN is a logic 0, MOSFETs MP21 and MP22 are conducting, and operate roughly like closed switches, coupling the drain and source. Since MOSFETs MP21 and MP22 are conducting, the drain and source of MOSFET MP21 are coupled to each other, the drain and source of MOSFET MP22 are coupled to each other, and accordingly the drain of MOSFET MP21 is coupled to the source of MOSFET P22. Accordingly, when signal IN is a logic 0, transistors MP21 and MP22 conduct or connect node PUP to node OUT. However, the gate of MOSFET MP21 (node P1) and the gate of MOSFET MP22 (node 5) are isolated from each other

when signal IN is at logic 0. As is well known in the art, in a MOSFET (such as MOSFETs MP21 and MP22 of Nebel), there is an insulator such as silicon dioxide separating the gate of the MOSFET from the drain and source of the MOSFET, so that substantially no conduction occurs between the gate of the MOSFET and its source or between the gate of the MOSFET and its drain. Accordingly, transistors MP21 and MP22 of Nebel do not connect or conduct node P1 to node N5.

In constrast, Applicant's Claim 10 recites, "the first shunt circuit is configured to short the first bias node to the high-range node if the full-range signal corresponds to a logic low". For at least these reasons, Applicant's Claim 10 is respectfully submitted to be allowable, and notice to that effect is earnestly solicited.

Similarly, in Nebel, when signal IN corresponds to a logic 1, node 6 is not conducted or connected to node N1. In contrast, Applicant's Claim 1 as amended recites, "the second shunt circuit is arranged to short the low-range node to the second bias node if a voltage associated with the full-range node corresponds to a logic high". For at least these reasons, Applicant's Claim 1 as amended is respectfully submitted to be allowable, and notice to that effect is earnestly solicited.

Applicant's Claim 9 is respectfully submitted to be allowable at least for the reasons stated above with regard to Claim 10.

Claims 3-5 and 12 are respectfully submitted to be allowable at least because they depend on Claim 1, which is submitted to be allowable. Claims 17-19 are respectfully submitted to be allowable at least because they depend on Claim 10, which is proposed to be allowable.

Rejection to Claim 2

The rejection to Claim 2 is respectfully traversed. Claim 2 is respectfully submitted to be allowable at least because Nebel does not disclose "the first bias node and the second bias node have approximately the same voltage", as recited in Applicant's Claim 2.

The Office Action states, with regard to the circuit illustrated in Fig. 1 of Nebel, "the first bias node (5) and the second bias node (6) have approximately the same voltage (2.5 Volts)". Applicant respectfully disagrees.

Terminal 5 of Nebel is at 1.4 V, a logic low voltage level sufficient to make PMOSFET MP22 conduct. Terminal 6 is at 3.6V, a log high voltage level sufficient to make NMOSFET

MN22 conduct. This is based on an N-well process, the wells being put at 5V and the substrate being put at 0V. See Col. 8, lines 37-42 of Nebel. If a voltage of 3.6V were place at terminal 5 and a voltage of 1.4V were placed at terminal 6, neither transistor MP22 nor transistor MN22 would conduct. Terminal 5 is at a logic low value of 1.4V, rather than being close to 2.5V, since 2.5V is a mid-voltage level rather than a logic low level. Terminal 6 is at a logic high value of 3.6V rather than being close to 2.5V, since 2.5V is a mid-voltage level rather than a logic high level. Accordingly, terminals 5 and 6 of Nebel do not have approximately the same voltage.

In contrast, Applicant's Claim 2 recites, "the first bias node and the second bias node have approximately the same voltage". For at least these reasons, Applicant respectfully submits that Claim 2 is allowable, and notice to that effect is earnestly solicited.

Rejection to Claims 8 and 11

Claims 8 and 11 have been re-written in independent form. The rejection to Claims 8 and 11 are respectfully traversed.

First, Claim 8 is respectfully submitted to be allowable for the reasons stated with regard to Claim 1 above. Second, claim 8 is respectfully submitted to be allowable at least because Nebel does not disclose, "the first shunt circuit is configured to influence a resistance between the first bias node and the high-range node depending on a full-range signal", as submitted in Applicant's Claim 8.

The Office Action states, "Nebel further teaches the inut level transistor circuit of claim 1, wherein the first shunt circuit (MP21-MP22) is configured to influence a resistance between the first bias node (5) and the high-range node (P1) depending on a full-range signal (IN)". Applicant respectfully disagrees.

In Nebel, transistor MP21 is configured to influence a resistance between the drain and source of MOSFET MP21 depending on signal IN. However, transistor MP21 does not influence a resistance between the gate of MOSFET MP21 (node P1) and the gate of MOSFET MP22 (node 5) based on signal IN. As is well known in the art, a MOSFET includes an insulator such as silicon dioxide between the gate and the source of the MOSFET, and between the gate and drain of the MOSFET. In Nebel, the resistance from the gate of transistor MP21 to the source of transistor

MP21 is Hi Z regardless of the voltage of signal IN. Accordingly, transistor MP21 does not influence a resistance between node 5 and node P1 based on signal IN.

In contrast, Applicant's Claim 8 recites, "the first shunt circuit is configured to influence a resistance between the first bias node and the high-range node depending on a full-range signal". For at least these reasons, it is respectfully submitted that Claim 8 is allowable, and notice to that effect is earnestly solicited. Claim 11 is respectfully submitted to be allowable for reasons analogous to those stated with regard to Claim 8 above.

Rejection to Claims 13-16 and 20

Claims 13 and 20 are not amended for reasons related to patentability, but are amended to comply with the intervening change in case law presented by SuperGuide Corporation v. DirecTV Enterprises, Inc., et al., 358 F.3d 870 (Fed. Cir. 2004).

Applicant respectfully submits that Claim 13 is allowable at least because Nebel does not disclose "ensuring that at least one of: the low-range node is driven during a full cycle of the full-range signal, or the high-range node is driven during the full cycle of the full-range signal", as recited in Applicant's Claim 13.

In Nebel, when signal IN is logic 0, node P1 is floating. Accordingly, node P1 is not driven when signal IN is logic 0.

Simiarly, in Nebel, when signal IN is logic 1, node N1 is floating. Accordingly, node N1 is not driven when signal IN is logic 1. In contrast, Applicant's Claim 13 recites, "ensuring that at least one of: the low-range node is driven during a full cycle of the full-range signal, or the high-range node is driven during the full cycle of the full-range signal".

The Office Action states, on page 9, "Regarding claims 13 and 20, the Examiner believes that Nebel inherently teaches the ensuring that at least one of: the low-range node is driven during a full cycle of the full-range signal, and the high-range node is driven during the full cycle of the full-range signal because the structure of Nebel in Fig. 1 is basically the same as the structure of the Applicant in Fig. 2; with the exception of diodes MP11 and MN11." The Office Action further states, "Since the circuit of Neble in Fig. 1 has the same electrical property of the Applicant's circuit in Fig. 2, Nebel teaches the ensuring that at least one of: the low-range node is driven during a full

cycle of the full-range signal, and the high-range node is driven during the full cycle of the full-range signal."

However, Applicant's circuit in Fig. 2 does not meet the limitations of Applicant's Claim 13. On page 3, Col. 27-29, Applicant's specification states, "The gates of transistors M3 and M4 are only actively driven during half of a cycle associated with the voltage level of the full range signal." Accordingly, the circuit of Applicant's Fig. 2 explicitly fails to the meet the limitation of Applicant's Claim 13 of "ensuring that at least one of: the low-range node is driven during a full cycle of the full-range signal, or the high-range node is driven during the full cycle of the full-range signal".

Nebel's circuit of Fig. 1 does not meet the limitation of "ensuring that at least one of: the low-range node is driven during a full cycle of the full-range signal, or the high-range node is driven during the full cycle of the full-range signal" because, like Applicant's circuit in Fig. 2, the gates of transistors MP21 and MN21 of Nebel are only actively driven during half of a cycle associated with the voltage level of signal IN.

For at least these reasons, it is respectfully submitted that Claim 13 is allowable, and notice to that effect is earnestly solicited.

Claims 14-16 are respectfully submitted to be allowable at least because they depend on Claim 13, which is proposed to be allowable. Claim 20 is respectfully submitted to be allowable at least for reasons analogous to those started with regard to Claim 13 above.

Conclusion

It is respectfully submitted that each of the presently pending claims (Claims 1-20) are in condition for allowance and notification to that effect is requested. The Examiner is invited to contact Applicant's representative at the below-listed telephone number if it is believed that prosecution of this application may be assisted thereby. Although certain arguments regarding patentability are set forth herein, there may be other arguments and reasons why the claimed invention is patentably distinct. Applicant reserves the right to raise these arguments in the future.

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Respectfully submitted,

By _____
Matthew M. Gaffney
Registration No.: 46,717
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257
(206) 262-8900
(212) 527-7701 (Fax)
Attorneys/Agents For Applicant

Customer No.: 38845

Attachments